WHAT IS CLAIMED IS:

1. An insulated-gate type semiconductor device in which a conductive layer for a gate is embedded into a trench which is formed in a semiconductor substrate, and a conductive layer for a source is provided on a major surface of said semiconductor substrate, wherein:

a portion of a gate pillar which is constituted by both said conductive layer for said gate and a cap insulating film for capping an upper surface of said conductive layer for said gate is projected from the major surface of said semiconductor substrate;

a side wall spacer is provided on a side wall of said projected portion of the gate pillar; and

said conductive layer for said source is connected to a contact region of the major surface of the semiconductor substrate, which is defined by said side wall spacer.

2. An insulated-gate type semiconductor device in which said conductive layer for said source is embedded into a trench which is formed in a semiconductor substrate, and said conductive layer for said source is provided on a major surface of said semiconductor substrate, wherein:

a portion of a gate-portion conductor layer is projected from the major surface of said semiconductor substrate;

a side wall spacer is provided on both a side wall of said projected conductive layer and a side wall

of a cap insulating film for capping an upper surface of said conductive layer for said gate; and

said conductive layer for said source is formed in a source contact hole which is defined by said side wall spacer.

3. An insulated-gate type semiconductor device as claimed in claim 1 wherein:

said conductive layer for said gate is made of polycrystal silicon containing an impurity; and

said conductive layer for said source is made of a metal which contains aluminium as a major component.

4. An insulated-gate type semiconductor device comprising:

a first semiconductor region selectively formed in a semiconductor substrate;

a second semiconductor region selectively formed in said first semiconductor region;

a trench which is reached from a major surface of said second semiconductor region to said semiconductor substrate; and

a conductive layer which is formed via an insulating film in said trench; wherein:

a gate pillar which is constituted by said conductive layer and a cap insulating film for capping an upper surface of said conductive layer owns a pillar which is elongated on a major surface of said second semiconductor region;

a side wall spacer is provided on a side wall of the pillar of said gate pillar;

an electrode is connected to said second semiconductor region in a contact region which is defined by said side wall spacer; and

said semiconductor substrate is used as a drain, said conductive layer is used as a gate, and said second semiconductor region is used as a source.

5. An insulated-gate type semiconductor device comprising:

a first semiconductor region selectively formed in a semiconductor substrate;

a second semiconductor region selectively formed in said first semiconductor region;

a trench which is reached from a major surface of said second semiconductor region to said semiconductor substrate; and

a conductive layer which is formed via an insulating film in said trench; wherein:

a portion of said conductive layer owns a pillar which is elongated on a major surface of said second semiconductor region;

a side wall spacer is provided on both a side wall of the pillar of said conductive layer and also a side wall of a cap insulating film for capping an upper surface of said conductive layer;

an electrode is connected to said second semiconductor region in a contact hole formed in a

contact region which is defined by said side wall spacer; and

said semiconductor substrate is used as a drain, said conductive layer is used as a gate, and said second semiconductor region is used as a source.

6. An insulated-gate type semiconductor device as claimed in claim 4 wherein:

said conductive layer which constitutes the gate is polycrystal silicon; and said insulating film is a thermal oxide film.

7. An insulated-gate type semiconductor device comprising:

a first conductivity type semiconductor main body;

a second conductivity type first semiconductor region formed at a predetermined depth within one major surface of said semiconductor main body, said second conductivity type being opposite to said first conductivity type;

a first conductivity type second semiconductor region formed at a predetermined depth within said first semiconductor region;

a first trench which penetrates said first semiconductor region, and is reached from a major surface of said second semiconductor region to said semiconductor main body;

a pillar gate which is constituted by both a gate-purpose conductive layer embedded via an insulat-

ing film into said first trench and a cap insulating film for capping an upper surface of said gate-purpose conductive layer, and a portion of which pillar gate having a pillar portion projected from the major surface of said second semiconductor region; and

a first electrode which is electrically connected to said second semiconductor region in a region between a side wall spacer provided on a side wall of said pillar portion of the pillar gate, and said side wall spacer.

8. An insulated-gate type semiconductor device comprising:

a first conductivity type semiconductor main body;

a second conductivity type first semiconductor region formed at a predetermined depth within one major surface of said semiconductor main body, said second conductivity type being opposite to said first conductivity type;

a first conductivity type second semiconductor region formed at a predetermined depth within said first semiconductor region;

a plurality of first trenches which penetrates said first semiconductor region, and are reached from a major surface of said second semiconductor region to said semiconductor main body;

a conductive layer for a gate embedded via an insulating film into each of said first plural

trenches, and a portion of which said conductive layer for said gate owns a pillar portion projected from the major surface of said second semiconductor region;

side wall spacers provided on a side wall of said pillar portion and also a side wall of a cap insulating film for capping an upper surface of said pillar portion;

a plurality of second trenches which are made shallower than said first trenches, and are formed in such a manner that said second trenches are reached from the major surface of the second semiconductor region to said first semiconductor region between said side wall spacers located adjacent to each other; and

a first electrode which is embedded into each of said second trenches so as to be electrically connected to said first semiconductor region and said second semiconductor region, and which is commonly connected on said conductive layer for said gate.

9. An insulated-gate type semiconductor device as claimed in claim 7 wherein:

said conductive layer for said gate is made of polycrystal silicon containing an impurity;

said first electrode is made of a metal which contains aluminium as a major component; and

said second electrode is made of a metal material different from said metal material of the first electrode.

10. An insulated-gate type semiconductor device

as claimed in claim 7 wherein:

said second electrode is formed on another major surface of said semiconductor main body, which is located opposite to said major surface thereof; and

said second electrode is made of either a metal layer in which nickel, titanium, nickel, and silver are sequentially stacked, or another metal layer in which titanium, nickel, and gold are sequentially stacked.

11. An insulated-gate type semiconductor device as claimed in claim 10 wherein:

said first electrode is a source electrode; and said second electrode is a drain electrode.

12. An insulated-gate type semiconductor device as claimed in claim 7 wherein:

said first trenches are formed in a stripe shape in such a manner that a side surface of said first semiconductor region constitutes either a crystalline surface (100) or a surface equivalent to said crystalline surface (100), and carriers are moved along either said crystalline surface (100) or said surface equivalent to said crystalline surface (100) by an electric field of said conductive layer for said gate.

13. An insulated-gate type semiconductor device as claimed in claim 7 wherein:

a field insulating film is formed on a portion of the major surface of said semiconductor main

body;

an extension portion of said conductive layer for said gate is provided on a portion of said field insulating film; and

a third electrode made of the same material as that of said first electrode is connected to said extension portion of said conductive layer for said gate.

14. An insulated-gate type semiconductor device as claimed in claim 13 wherein:

a back-to-back protective element which is electrically connected between said first electrode and said third electrode is provided on another portion of said field insulating film.

15. An insulated-gate type semiconductor device having a longitudinal structure, comprising:

a semiconductor main body indicative of a first conductivity type;

a first semiconductor region indicative of a second conductivity type, which is formed in said semiconductor main body;

a second semiconductor region indicative of the first conductivity type, which is formed in said first semiconductor region; and

a trench gate which is reached from a major surface of said second semiconductor region to the region of said semiconductor main body; wherein:

a portion of a gate pillar which is made of

both said trench gate and an insulating film for covering an upper surface of said trench gate exceeds and is projected from the major surface of said second semiconductor region;

a side wall spacer is provided on a side wall of said projected gate pillar; and

a source electrode connected to said semiconductor region is provided on a contact region defined by said side wall spacer.

16. An insulated-gate type semiconductor device having a longitudinal structure, comprising:

a semiconductor main body indicative of a first conductivity type;

a first semiconductor region indicative of a second conductivity type, which is formed in said semiconductor main body;

a second semiconductor region indicative of the first conductivity type, which is formed in said first semiconductor region; and

a trench gate which is reached from a major surface of said second semiconductor region to the region of said semiconductor main body; wherein:

a portion of said trench gate exceeds and is projected from the major surface of said second semiconductor region;

a side wall spacer is provided on both said projected trench gate and a side wall of an insulating film for covering an upper surface of said trench gate;

and

a source electrode connected to said semiconductor region is provided in a contact hole defined by said side wall spacer.

17. An insulated-gate type semiconductor device as claimed in claim 15 wherein:

said side wall is formed via a thermal oxidation film which is formed on a surface of the projected portion of said trench gate.

18. A method for manufacturing an insulated-gate type semiconductor device in which a gate-purpose conductive layer is embedded into a trench which is formed in a semiconductor substrate, and a source-purpose conductive layer is provided on said major surface, comprising:

a step for forming a first semiconductor region within said semiconductor substrate;

a step for forming a trench in said semiconductor substrate in such a manner that said trench penetrates said first semiconductor forming region;

a step for forming a gate insulating film on a surface of said first semiconductor region which is exposed within said trench;

a step in which the trench where said gate insulating film is formed by a gate pillar made of both said gate-purpose conductive layer and a cap insulating film for capping an upper surface of said gate-purpose conductive layer, and a portion of said gate pillar is

projected from the major surface of said semiconductor substrate;

a step for forming a second semiconductor region within said first semiconductor region which is segmented by said trench;

a step for forming a side wall spacer on both said projected conductive layer and an insulating film for covering an upper surface of said projected conductive layer; and

a step for forming said source-purpose conductive layer in a source contact region defined by said side wall spacer.

19. A method for manufacturing an insulated-gate type semiconductor device in which a gate-purpose conductive layer is embedded into a trench which is formed in a semiconductor substrate, and a source-purpose conductive layer is provided on said major surface, comprising:

a step for forming a first semiconductor region within said semiconductor substrate;

a step for forming a plurality of trenches in said semiconductor substrate in such a manner that said trenches penetrate said first semiconductor forming region;

a step for forming a gate insulating film on a surface of said first semiconductor region which is exposed within each of said trenches;

a step in which each of said trenches where

said gate insulating film is formed is embedded, and a portion of said gate-purpose conductive layer which is projected to the major surface of the semiconductor substrate is formed;

a step for forming a second semiconductor region within said first semiconductor region which is segmented by said trenches;

a step for forming a side wall spacer on both said projected conductive layer and an insulating film for covering an upper surface of said projected conductive layer;

a step for forming a contact hole in a source contact region defined by said side wall spacer; and

a step for forming said source-purpose conductive layer in said contact hole.

20. A method for manufacturing an insulated-gate type semiconductor device in which a gate-purpose conductive layer is embedded into a trench which is formed in a semiconductor substrate, and a source-purpose conductive layer is provided on said major surface, comprising:

a step for forming a first semiconductor region within said semiconductor substrate;

a step for forming a trench in said semi-conductor substrate in such a manner that said trench penetrates said first semiconductor forming region;

a step for forming a gate insulating film on a surface of said first semiconductor region which is

exposed within said trench;

a step in which the trench where said gate insulating film is formed by a gate pillar made of both said conductive layer for said gate and a cap insulating film for capping an upper surface of said conductive layer for said gate, and a portion of said gate pillar is projected from the major surface of said semiconductor substrate;

a step for forming a second semiconductor region within said first semiconductor region which is segmented by said trench;

a step for forming a side wall spacer on both said projected conductive layer and an insulating film for covering an upper surface of said projected conductive layer;

a step for forming a contact hole in said second semiconductor region, while said side wall spacer is employed as a mask;

a step in which after said contact hole has been formed, the side wall spacer is moved backwardly by way of an etching back operation so as to expose a surface of the semiconductor substrate of said second semiconductor region; and

a step for forming said source-purpose conductive layer within both the exposed surface portion of the semiconductor substrate of said second semiconductor region and also said contact hole.